



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/721,000	01/03/2001	Bertil Brandin	P00.1982	3129

30596 7590 03/16/2004

HARNESS, DICKEY & PIERCE, P.L.C.
P.O.BOX 8910
RESTON, VA 20195

EXAMINER

SHECHTMAN, SEAN P

ART UNIT	PAPER NUMBER
----------	--------------

2125

DATE MAILED: 03/16/2004

17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/721,000

Applicant(s)

BRANDIN ET AL.

Examiner

Sean P. Shechtman

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination. Claims 1 and 4-8 have been amended.
Claims 9-16 have been added.

Drawings

2. Objections withdrawn due to the amendment.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5, 9, 13, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 13 are directed toward at least one of limitations: “an individual process is blocked...” (A) and “an individual process reaches an unauthorized...” (B). Therefore, it is unclear whether the claim limitations include A, B, or (A and B). For purposes of examination, it will be assumed that the limitations include A or B.

Claims 9 and 16 are directed toward at least one of limitations: “that there are no impediments...” (C) and “that each of said individual processes occupies...” (D). Therefore, it is unclear whether the claim limitations include C, D, or (C and D). For purposes of examination, it will be assumed that the limitations include C or D.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Art Unit: 2125

4. Claims 1-4, 7, 8, 10-12, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat No. 5,452,461 to Umekita.

Referring to claims 1 and 8, Umekita discloses a method/apparatus for designing a control of a complete process which comprises a number of individual processes (Col. 24, lines 34-39, Umekita clearly teaches a method of designing the control of a computer by compiling a source program into object programs for parallel processing by a multi-processor system), said method comprising the steps of:

Identifying functionalities of said individual processes (Col. 22, lines 20-24); Performing a validation by automatically verifying future interplay of said functionalities (Col. 22, lines 25-29) in accordance with an input to said complete process (Fig. 1, element 1) and producing a validation result (Col. 22, lines 30-34); and determining data for future controlling of said complete process from said validation result (Col. 22, lines 39-44; Col. 8, lines 6-51).

Referring to claims 2 and 10, Umekita discloses the method/apparatus above further comprising the step of performing a sequence optimization (Col. 22, lines 30-34).

Referring to claims 3 and 11, Umekita discloses the method/apparatus above further comprising the step of producing data for the future control in an executable code from (Col. 22, lines 44-46).

Referring to claims 4 and 12, Umekita discloses the method/apparatus above further comprising the step of controlling individual affected processes by a software unit which is one of said functionalities of said individual processes (Col. 24, lines 34-39).

Referring to claims 7 and 15, Umekita discloses the method/apparatus above further comprising the step of controlling a technical installation with data determined for controlling said complete process (Col. 5, lines 1-14).

5. Claims 1-5, 7-13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat No. 5,584,019 to Kikuchi.

Referring to claims 1 and 8, Kikuchi discloses a method/apparatus for designing a control of a complete process which comprises a number of individual processes (Col. 1, lines 13-19; Col. 32, 52-56), said method comprising the steps of:

Identifying functionalities of said individual processes (Col. 32, lines 56-62; Col. 10, lines 42-67); Performing a validation by automatically verifying future interplay of said functionalities (Col. 33, lines 8-14; Col. 33, lines 27-34; Col. 23, lines 1-12; Col. 1, lines 13-16) in accordance with an input (Col. 32, lines 663-64; Col. 3, lines 17-24) to said complete process and producing a validation result (Col. 33, lines 14-26); and determining data for future controlling of said complete process from said validation result (Col. 33, lines 18-22).

Kikuchi teaches the design of a control system (See all claims; Col. 2, lines 35-52; Col. 1, lines 33-36) capable of controlling in parallel a plurality of processing portions each of which has an individual function or soft modules acting in association as a system (Col. 1, lines 13-16). Storage means stores state of control and control sequence for each processing element (Col. 3, lines 39-42). Determining means determines whether a system transition between the present system state and the next system state candidate is permitted with respect to the transition in the processing element contained in the system transition on the basis of information on restriction

Art Unit: 2125

(Col. 33, lines 8-14), wherein Kikuchi goes on to teach said restrictions comprise restrictions according to a state or a transition in one of the other processing elements... (Col. 33, claims 2-3).

Referring to claims 2 and 10, Kikuchi discloses the method/apparatus above further comprising the step of performing a sequence optimization (Col. 15, lines 46-50).

Referring to claims 3 and 11, Kikuchi discloses the method/apparatus above further comprising the step of producing data for the future control in an executable code from (Col. 25, lines 12-45 Col. 33, lines 14-16; Fig. 46, element 50).

Referring to claims 4 and 12, Kikuchi discloses the method/apparatus above further comprising the step of controlling individual affected processes by a software unit which is one of said functionalities of said individual processes (Col. 1, lines 13-16).

Referring to claims 5 and 13, Kikuchi teaches the method/apparatus above wherein said validation result can indicate that one or more of said individual processes is an impeding process, an impeding process being defined as an individual process that reaches an unauthorized state endangering operation of said complete process (Col. 1, lines 21-37; Col. 2, lines 3-26; Col. 3, lines 6-11; Cols. 39-40, claim 22).

Referring to claims 7 and 15, Kikuchi discloses the method/apparatus above further comprising the step of controlling a technical installation with data determined for controlling said complete process (Col. 1, lines 18-19).

Referring to claims 9 and 16, Kikuchi discloses the method/apparatus above wherein a successful type of validation result indicates that each of said individual processes occupies an authorized state (Cols. 39-40, claim 22; Col. 1, lines 21-37).

6. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat No. 6,009,454 to Dummermuth.

Referring to claims 1 and 8, Dummermuth discloses a method/apparatus for designing a control of a complete process which comprises a number of individual processes (Abstract; Col. 2, lines 42-47; Col. 9, lines 45-48; Col. 10, lines 15-19), said method comprising the steps of:

Identifying functionalities of said individual processes (Col. 10, lines 20-21); Performing a validation by automatically verifying future interplay of said functionalities (Col. 8, line 66- Col. 9, line 12; Abstract; Fig. 2, Col. 5, line 54 – Col. 6, line 5) in accordance with an input to said complete process and producing a validation result (Col. 9, lines 13-17); and determining data for future controlling of said complete process from said validation result (Col. 8, lines 15-49; Col. 3, lines 36-39).

Dummermuth teaches designing the control of a complete industrial process by breaking down an industrial control program into smaller tasks (Col. 2, lines 42-47; Col. 9, lines 45-48; Col. 10, lines 15-19). Dummermuth teaches identifying a fixed number of instructions in each task to be executed without interruption (Col. 10, lines 20-21). Dummermuth performing a validation by automatically verifying future interplay of said functionalities because Dummermuth clearly teaches the ability to execute separate tasks in an apparently simultaneous fashion to control the number of instructions in each task so that a given task may be ensured complete execution prior to task switching (i.e., prior to future interplay). This permits tasks to be linked by writing linking tasks to coordinate two other tasks (Col. 8, line 66- Col. 9, line 12).

Art Unit: 2125

Dummermuth goes on to give an example in col. 9, lines 5-12. This is done in accordance with a control program input by a programmer (Col. 5, lines 5-10).

Referring to claims 2 and 10, Dummermuth discloses the method/apparatus above further comprising the step of performing a sequence optimization (Col. 6, lines 16-25).

Referring to claims 3 and 11, Dummermuth discloses the method/apparatus above further comprising the step of producing data for the future control in an executable code from (Col. 5, lines 5-13).

Referring to claims 4 and 12, Dummermuth discloses the method/apparatus above further comprising the step of controlling individual affected processes by a software unit which is one of said functionalities of said individual processes (Col. 7, lines 23-34).

Referring to claims 5 and 13, Dummermuth teaches the method/apparatus above wherein said validation result can indicate that one or more of said individual processes is an impeding process, an impeding process being defined as an individual process that reaches an unauthorized state endangering operation of said complete process (Col. 9, lines 28-35).

Referring to claims 6 and 14, Dummermuth teaches the method/apparatus above further comprising the step of controlling individual processes of an automatic placement machine (Figs. 1 and 2; Col. 5, lines 13-28).

Referring to claims 7 and 15, Dummermuth discloses the method/apparatus above further comprising the step of controlling a technical installation with data determined for controlling said complete process (Col. 4, lines 48-51).

Art Unit: 2125

Referring to claims 9 and 16, Dummermuth discloses the method/apparatus above wherein a successful type of validation result indicates that each of said individual processes occupies an authorized state (Col. 9, lines 28-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,584,019 to Kikuchi as applied to claims 1 and 8 above, and further in view of U.S. Pat. No. 4,579,444 to Pinckney. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,452,461 to Umekita as applied to claims 1 and 8 above, and further in view of U.S. Pat. No. 4,579,444 to Pinckney.

Referring to claims 6 and 14, Kikuchi teaches the method/apparatus above further comprising the step of controlling individual processes of a printer or copying machine (Col. 1, lines 16-19 of '019). Kikuchi fails to teach that the printer or copier is an automatic placement machine.

Referring to claims 6 and 14, Umekita fails to teach the method/apparatus above further comprising the step of controlling individual processes of an automatic placement machine.

However, referring to claims 6 and 14, Pinckney teaches analogous art, wherein a copier machine is an automatic placement machine (Cols. 25-26, claim 14 of '444) with plural individual processes (Col. 23, line 43 – Col. 28, line 30 of '444).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teaching of Kikuchi or Umekita with the copier machine of Pinckney.

One of ordinary skill in the art would have been motivated to combine these references because Pinckney teaches a copier machine is an automatic placement machine (Cols. 25-26, claim 14 of '444), and Pinckney teaches an improved method and apparatus for automatically feeding and registering individual document sheets to be copied on a copier platen (Col. 1, lines 4-8 of '444). Furthermore, Pinckney teaches stopping a fed document without using a mechanical registration stop (Col. 8, lines 24-27 of '444). Further still, Pinckney teaches automatically changing optical ratio or paper size (Col. 22, lines 39-40 of '444).

Response to Arguments

8. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents or publications are cited to further show the state of the art with respect to simulating the future interplay of functionalities of individual processes that make up a

Art Unit: 2125

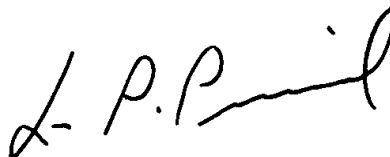
complete process and producing a validation result for a future ASIC for future control of the complete process.

U.S. Pat. No. 5,764,948 to Le Van Suu (Col. 1, lines 6-20; Col. 2, lines 6-10; Col. 3, lines 1-17; Fig. 2; Col. 7, lines 8-34).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (703) 305-7798. The examiner can normally be reached on Monday-Friday from 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard, can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.



SPS

Sean P. Shechtman

March 6, 2004

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100